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PSPWM BASED SCMLI TOPOLOGY WITH A REDUCED NUMBER OF SWITCHES FOR AC POWER DISTRIBUTION SYSTEM

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Abstract: The main aim of this project is Phase Shift Pulse Width Modulation (PSPWM) based Switched Capacitor Multi Level Inverter (SCMLI) topology with a reduced number of switches for AC power distribution system. The output voltage and current waveforms from the various PV sources are being produced by the power electronics converters. In recent years, PV applications have concentrated on the delivery of high-frequency AC electricity. With DC/AC SCMLIs, for example, the number of power conversion stages and components is greatly reduced resulting in an increased rate of conversion. A new PSPWM based SCMLI topology with fewer switches and a self-balanced floating capacitor (FC) voltage is proposed in this project. A single dc source and three dc sources make up the suggested topology. With the proposed design, a voltage output (Vo) that is twice as high as the input voltage can be generated (Vin). Compared to other topologies recently proposed, this one has a faster discharge time. In addition, the voltage stress on switches is les in relation to the load voltage. The proposed simulation results are studied in MATLAB/SIMULINK environment.

Keywords: PS-PWM, Multilevel inverter, Frequency AC power distribution, Floating capacitor

I.INTRODUCTION

Since there is a huge need for electric power and infinite solar energy sources, PV-fed applications are growing at an ever-increasing rate. As a result, additional PV applications with high power conversion efficiency will be possible thanks to power electronics. High-frequency power distribution systems, such as space, communications, and computer applications, can benefit from the combination of PV with power electronics technologies [1]-[2]. Electrical systems for aeroplane applications with high-frequency AC loads are depicted in the figure to the right. In terms of power converters for medium to large-scale PV systems, the multilayer inverters (MLIs) are well established and dominant. The MLI's key advantages are its low dv/dt and lower overall harmonic distortion (THD). In addition to the AC drives, FACTS devices, renewable energy, and microgrids, MLI can be used in a wide range of other applications. Cascaded h-bridge, neutral point clamped, and flying capacitor topologies are commonly referred to as MLIs in the literature. High-voltage and high-power applications are better suited for these typical topologies [3]. Despite the low dv/dt stress of these topologies, the number of switches, diodes, and dc-link capacitors or dc sources is large. It is proposed in [4] that a new MLIs topology consumes fewer power components with less stress. However, these topologies are able to reduce the number of switches, but the dv/dt stress they generate is substantial. In addition, the SCMLIs are added in [5]-[15] to reduce the burden on switches and switch count. Topologies using SCMLI topologies are more appropriate for producing high voltage levels with fewer switches. Furthermore, these topologies provide a single dc supply and low dv/dt stress. The FC is utilised in accordance with the number of voltage levels required.

The cascaded structure is suggested for those who want to go even deeper into the hierarchical structure. Compared to the input voltage, the output voltage gain is two times greater. Additionally, new SCMLI topologies with a voltage gain of 1:2 are advocated for 9L in [11]-[13] to reduce switch count and switch voltage stress. However, these topologies only work with a 9L output voltage waveform, thus the cascaded topology is the preferred alternative if you want to go even farther. SCMLI topology for 13L inverter has been presented in [14]-[18] as a way to avoid this. With a voltage gain of 1:2 and a cascaded structure once

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more recommended for higher voltages, the basic unit in [14] employs two DC sources to generate the 13L. Similar to the topologies in [15] - [18], additional switches and FCs are required for these designs. Crisscrossed structures with self-voltage balancing and boosting capabilities are shown in [15]. Aside from that, the switch has a high component count and voltage stress. There is a 13L-SCMLI with a gain of six Vin [16]. There are 13 switches, 2 diodes, and 3 FCs involved in the design of this network. In [17] and [18], the dual supplied 13L inverter is shown. Six times as much voltage is output, yet the overall component has been increased. As in [18], there is no way to use a single dc source in this case. Although the voltage gain is 1.5 vin with more components in [19], the new 'K' type generalised SCMLI topology has a lower power component.

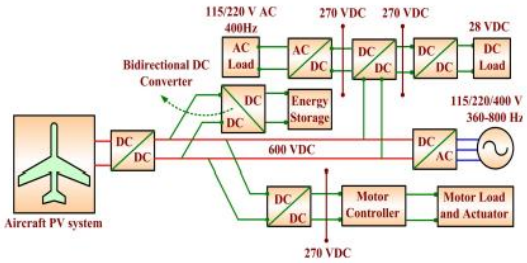

Fig. 1. Typical aircraft electric system without auxiliary source.

It is possible to use a single dc source with dc-link capacitors in the suggested topology, but three series connected dc sources are also possible. [20] presents numerous multi-source MLIs with reduced switch count, which have the following benefits: In order to achieve multilevel output first stage, the source-side cell, which connects the sources in various combinations, is used. In order to extend the topology for a higher number of voltage sources, the topology could be extended to generate a higher number of voltage levels with fewer components. In order to extend the topology for a higher number of voltage sources, the topology could generate a higher number of voltage levels with fewer components. As a primary downside, the switches' voltage stress is greater than half of the output voltage in these topologies. This work presents a novel 13L-SCMLI topology with a lower number of switches and voltage stress on the switch in order to alleviate these shortcomings. Using a single dc source with a smaller FC number, it is possible to generate a greater number of voltage levels. It is also recommended that the charging period of the FC be longer than the discharging time. There are several advantages to the proposed topology, including I the proposed topology generates the 13L output voltage level with one dc source and a reduced number of switches, (ii) dv/dt stress is equal to the Vin, (iii) it has a selfvoltage balancing and two times boosting ability, (iv) a single FC is used, and the charging time is longer than the discharging time, and (v) it has a selfvoltage balancing and two times boosting capacity (v) The voltage ratings of the front-end dc/dc converter have been decreased. A Nearest Level Modulation (NLM) is employed to generate the switching pulses necessary in this work. Low switching loss and ease of implementation in a digital controller are two of its advantages. As shown in [22], the typical NLM selects the output voltage level that is closest to the reference. dc-offset of 0.25 is used in the improved Nearest Level Control (NLC). There is also an increase in RMS value as a result of this. The greater voltage THD is found at fewer voltage levels, as can be seen. It is shown in [24] that the highest dc loss can be avoided by using a dc-offset value of 0.40 with a maximum loss of 0.4Vin.

II. PROPOSED 13 LEVELS INVERTER CONFIGURATION

A. Proposed Circuit

Figure 2 depicts the planned 13L-SCMLI circuit diagram. V1=V2=V3= Vin and VFC is the voltage across the FC are three DC sources with the same magnitude, V1=V2=V3= Vin. Using four diodes or two anti-series IGBTs with anti-parallel diodes, the switches Sab and Sab' are bidirectional switches. There are three DC sources in Fig. 2(a), but only one source with three DC-link capacitors in Fig. 2(b) (b). A short circuit can be avoided by not turning on all four switches at the same time: SR (on), SSR (on), SSR' (on), and SSR' (on) all at the same time. All of the components of the cross

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connected (CCS) switching capacitor cell are present in this cell.

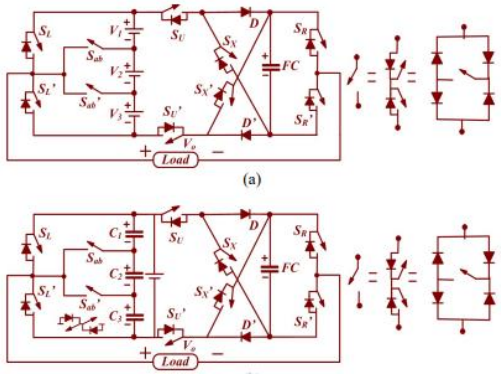

Fig. 2. High-frequency 13L inverter circuit diagram (a) multiple dc sources as input (b) a single dc source as input.

B. Switching pattern and modes of operation

As indicated in Fig. 3, there are a number of different modes of operation for the switch shown in Table I. According to Fig. 2(a), 13L's modes of operation are depicted, and a similar procedure can be applied to the other two figures (b). As illustrated in Fig. 3, the following states follows:

TABLE I. Switching pattern for proposed 13-level MLI

State	ON State Switches	DC Source		FC*	V_O
		Fig.2 (a)	Fig.2 (b)		
A	S_{ab}, S_U, D, S_R, S_U', D'	V_1	C_1	C	$+V_{in}$
B	S_{ab}', S_U, D S_R, S_U', D'	V_1+V_2	C_1+C_2	C	$+2V_{in}$
C	S_L', S_U, D, S_R, S_U', D'	$V_1+V_2+V_3$	$C_1+C_2+C_3$	C	$+3V_{in}$
D	S_{ab}, S_U, S_R, S_X	V_1	C_1	D	$V_{in}+V_{FC}$
E	S_{ab}', S_U, S_R, S_X	V_1+V_2	C_1+C_2	D	$2V_{in}+V_{FC}$
F	S_L', S_U, S_R, S_X	$V_1+V_2+V_3$	$C_1+C_2+C_3$	D	$3V_{in}+V_{FC}$
O	S_L, S_U, S_X, S_R' S_L', S_U', S_X', S_R	-	-	-	$0V_{in}$
A'	S_{ab}', S_U, D, S_R', S_U', D'	V_3	C_3	C	$-V_{in}$
B'	S_{ab}, S_U, D, S_R', S_U', D'	V_2+V_3	C_2+C_3	C	$-2V_{in}$
C'	S_L, S_U, D, S_R', S_U', D'	$V_1+V_2+V_3$	$C_1+C_2+C_3$	C	$-3V_{in}$
D'	S_{ab}', S_X', S_R', S_U'	V_3	C_3	D	$-V_{in}-V_{FC}$
E'	S_{ab}, S_X', S_R', S_U'	V_2+V_3	C_2+C_3	D	$-2V_{in}-V_{FC}$
F'	S_L, S_X', S_R', S_U'	$V_1+V_2+V_3$	$C_1+C_2+C_3$	D	$-3V_{in}-V_{FC}$

*State of FC, C-charging of FC, D-discharging of FC

State A: With all three dc power sources linked in series with the FC via the switches D, SU' and D', the FC is charged from 0 V to 3 Vin in this configuration. To generate the first voltage level of V1 (Vin) across the load, switches SR and Sab are activated.

State B: It is necessary to turn on the same set of switches as before (SU, D, SU' and D') in order to keep the FC voltage at 3 Vin (VFC=3 Vin), while Sab is left off. To find the voltage across the load, add together the voltages from the two dc sources: V1 and V2 (plus two Vin).

State C: In order to supply a maximum voltage of Vin across the load, the bottom DC source voltage is combined with V1 and V2. The FC is charged 3 Vin at this time. There are four switches for charging and two for loading: switches SU, D, SU', and D'. In the first three states, FC is charged on a regular basis. Each dc source is charging and discharging the FC in the next three stages.

State D: To discharge the FC in this state the switches SU, SR, and SX are all switched on. Across the load, V1+VFC (+Vin+VFC) is the voltage.

State E: It is set at +2 Vin +VFC with the switches SU, SU's, SR's, and SX on.

State F: Turn on the switches SL', SU, SR, and SX. Vo= +3 Vin +VFC is the voltage applied. The FC is charged and discharged at the same time, based on these comments. There are four duplicate states available at this point in the game. Switches SL, SU, D, and SR are all turned on with a charged FC in order to achieve a unity power factor. The FC is not charged when the power factor is out of balance.

State A' is changed to C' and discharged to F in the negative half cycle of the FC. Table I lists the switches that are activated during each stage. The pulses for switches are generated using the NLM approach as depicted in Fig. 4. As compared to standard SPWM, the NLM employs a fundamental frequency approach scheme that has low switching losses. These frequencies are 360, 400, and 1000 Hz, respectively. Further, the National Library of Medicine (NLM) is described as follows: Vref/VCons is the Modulation Index.

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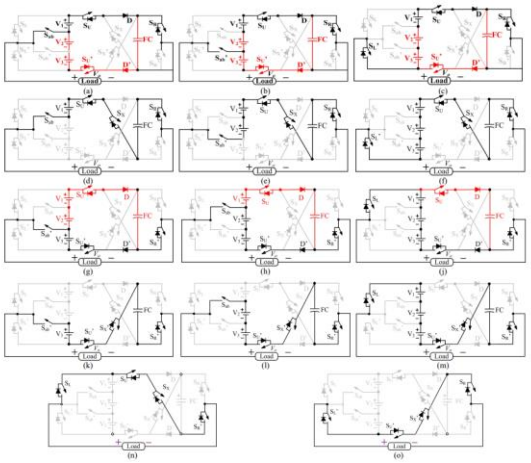

Fig. 3 Operation modes for each voltage level, (a)-(f) state A-F, (g)-(m) state A'-F', (n)-(o) state 0.

III. PROPOSED PSPWM TECHNQUIE

In PSPWM all the triangular carriers have the same frequency and same peak-peak amplitude. but there is a phase shift between any two adjacent carrier waves. From Voltage levels (m-1) carrier signals are required and they are phase shifted with an angle of θ=(360°/m-1). The gate signals are generated with proper comparison of carrier wave and modulating signal .

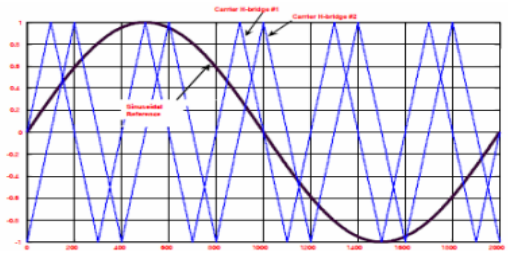

Fig. 4 Phase Shifted Carrier PWM

IV.SIMULATION RESULTS

TABLE 1. Parameters of 13-level MLI

Parameters	Ratings
I/P (Vdc)	100V
Load	R=100 Ohm, L=20 mH R=40 Ohm, L=2mH
IGBT	600V, 32A
O/P Freq.	F1=360Hz, F2=400Hz

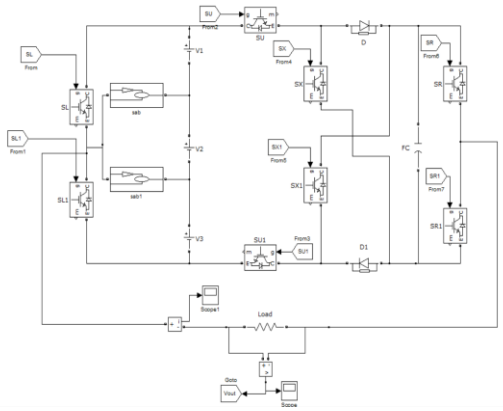

Fig.5 MATLAB/SIMULINK circuit diagram of the 13 level-MLI

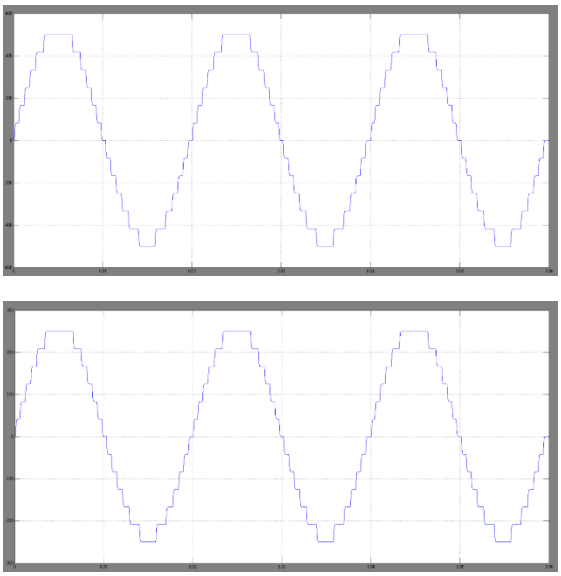

Fig.6 simulation result for R =100 Ω, 10A/div

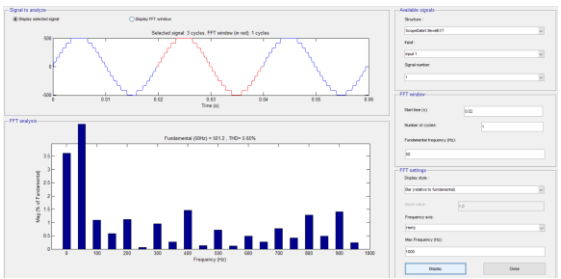

Fig.7 THD% of 13 level voltage is 5.65%

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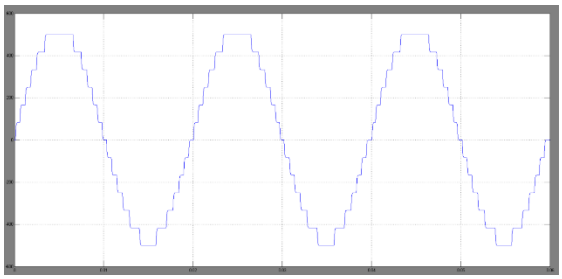


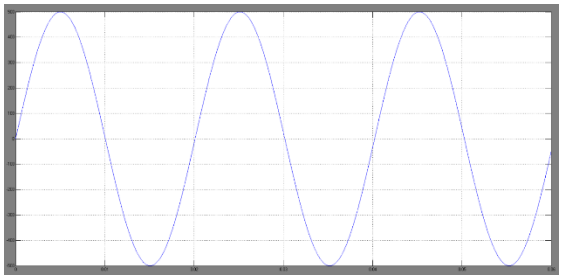


Fig.8 Output voltage and current waveforms for Load 1 at 360HZ

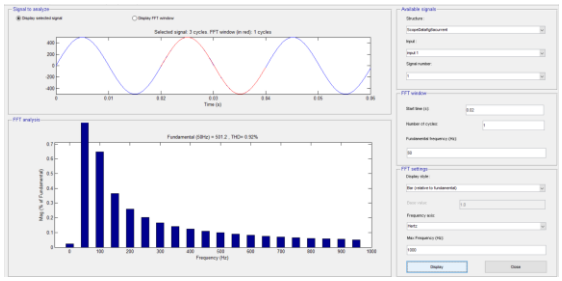
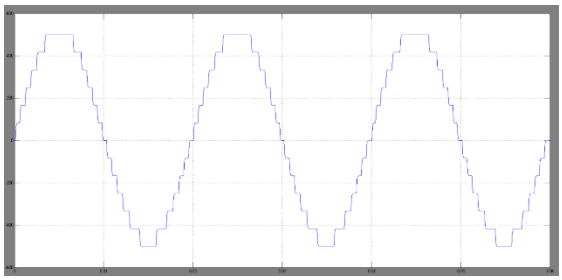


Fig.9 Output current THD (0.92%) at load 1 at 360HZ



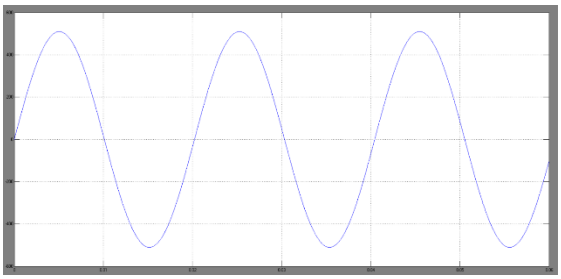


Fig.10 Output voltage and current waveforms for Load 2 at 360Hz

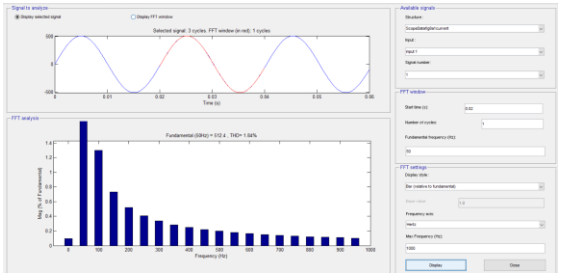
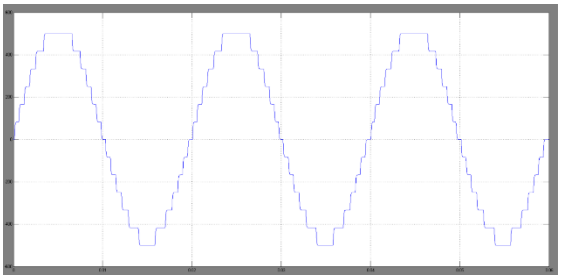


Fig.11 Output current THD (1.84%) at load 2 at 360HZ



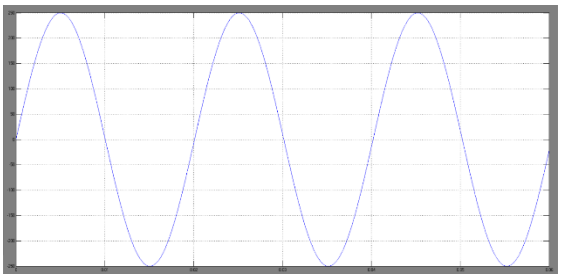


Fig.12 Output voltage and current waveforms for Load 1 at 400Hz

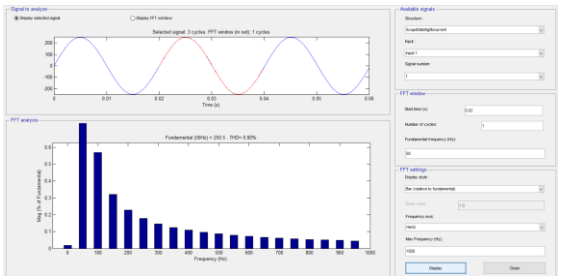


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Fig.13 Output current THD (0.80%) at load 1 at 400HZ

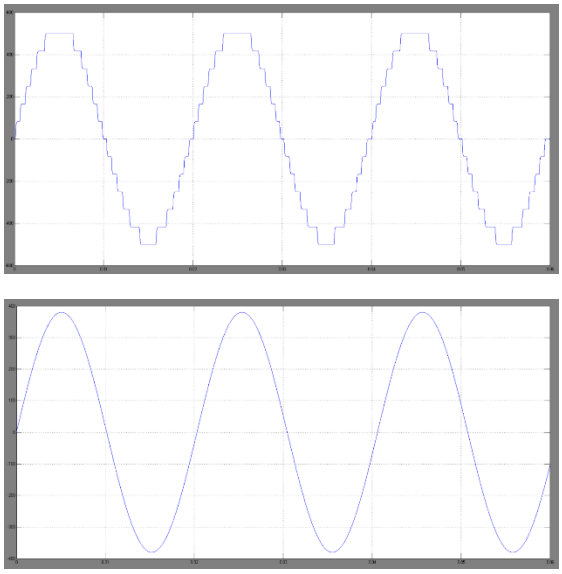


Fig.14 Output voltage and current waveforms for Load 2 at 400Hz

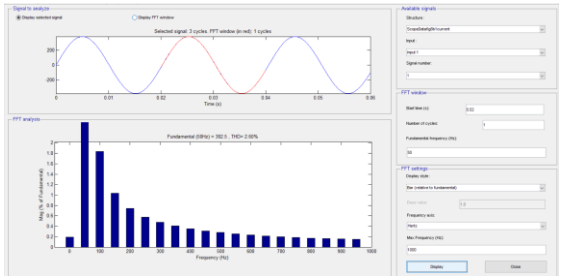
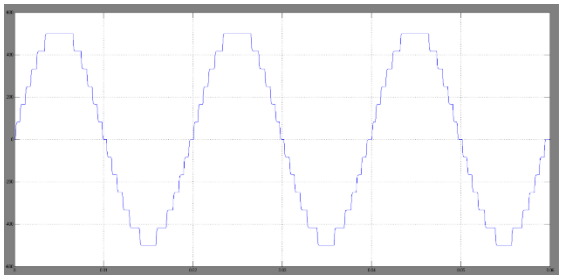


Fig .15 Output current THD (2.60%) at load 2 at 400HZ



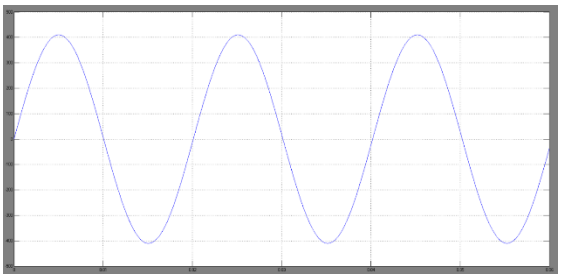


Fig.16 Output voltage and current waveforms for Load 1 at 1000Hz

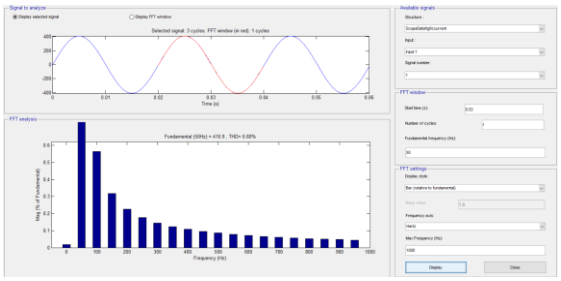
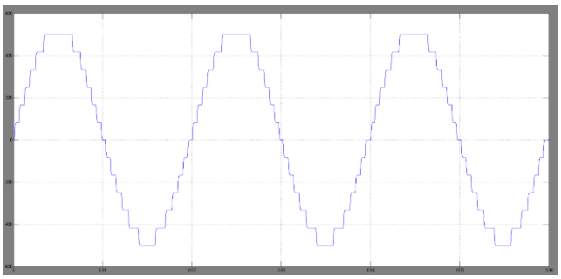


Fig.17 Output current THD (0.80%) at load 1 at 1000HZ



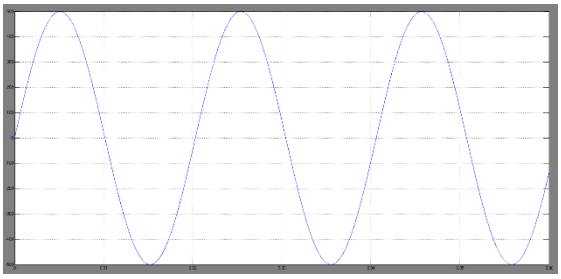


Fig.18 Output voltage and current waveforms for Load 2 at 1000Hz

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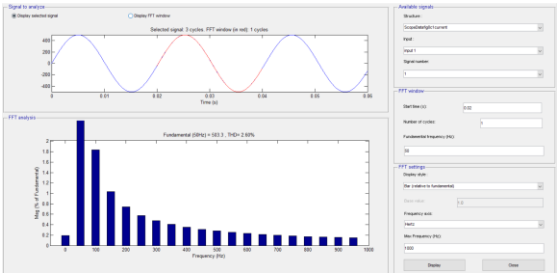

Fig.19 Output current THD (2.60%) at load 2 at 1000HZ

COMPARISION TABLE

	Existing System (THD%)	Proposed System (THD%)
Output voltage	**6.75%**	**5.65%**
Output current (Load1) at 360Hz	**1.07%**	**0.92%**
Output current (Load2) at 360Hz	**2.06%**	**1.84%**
Output current (Load1) at 400Hz	**0.96%**	**0.80%**
Output current (Load2) at 400Hz	**2.78%**	**2.60%**
Output current (Load1) at 1000Hz	**0.91%**	**0.80%**
Output current (Load2) at 1000Hz	**2.74%**	**2.60%**

CONCLUSION

A new PSPWM based 13L-SCMLI architecture with self-voltage boosting ability has been demonstrated. The suggested topology's major purpose is to reduce the number of switches with a self-balanced FC voltage. The proposed PSPWM based 13L-SCMLI topology has been compared with well-known contemporary topologies. It confirms that the proposed13L-SCMLI topology has not only decreased the number of switches but also has superior advantages in terms of FCs count, high voltage gain, and an equal number of cycles of charging and discharging of FCs. It should be mentioned that majority of the investigated topologies do not satisfy all these properties together. The proposed architecture was simulated and evaluated in the experimental setup operating at a fundamental frequency of 360 Hz, 400 Hz, and 1000 Hz. It confirms that both outcomes had a strong agreement in terms of THD and output power. The simulation efficiency is likewise almost close to experimental efficiency. The simulation results were provided for dynamic load fluctuations, where the power analysis is carried out for all three frequencies. The proposed topology has reached a maximum efficiency of 98% for 600W at unit power factor making it more suitable for high frequency power distribution applications like aviation

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